Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A fabrication method for integrating a plurality of heterogeneous circuit devices in a single substrate, comprising:

providing a substrate;

forming a first ion implantation protective layer over the substrate;

removing a portion of the first ion implantation protective layer to expose a first portion of the substrate;

ion implanting a high voltage well of a first circuit device in the first portion of substrate using the partially removed first ion implantation protective layer to allow ion implantation at the first portion;

forming a second ion implantation protective layer over at least the first portion of the substrate;

removing a second portion of the first ion implantation protective layer to expose a second portion of the substrate; and

ion implanting a first low voltage well of a second circuit device in the second portion of the substrate using the partially removed first ion implantation protective layer and the second ion implantation protective layer to allow ion implantation at the second portion.

2. (Original) The method of claim 1, further comprising ion implanting a photodiode in the substrate.

3. (Original) The method of claim 1, further comprising forming at least one microelectomechanical system-based element in the substrate.

4. (Original) The method of claim 1, wherein providing a substrate comprises providing a layer of silicon.

5. (Original) The method of claim 4, wherein providing a layer of silicon comprises providing a layer of p-type silicon.

6. (Original) The method of claim 1, wherein providing a substrate comprises providing a silicon-on-insulator wafer comprising a single-crystal-silicon layer, a substrate and an insulator layer therebetween.

7. (Original) The method of claim 6, wherein providing a silicon-on-insulator wafer comprises providing a silicon-on-insulator wafer comprising a p-type silicon layer, a substrate and an insulator layer therebetween.

8. (Currently Amended) The method of claim 1, further comprising:

forming a third ion implantation protective layer over the substrate;

removing a portion of the third ion implantation protective layer; and

ion implanting a second low voltage well of the second circuit device in the substrate using the partially removed third ion implantation protective layer to allow ion implantation.

9. (Original) The method of claim 8, further comprising forming a field oxide layer over at least part of each of the high voltage well, the first low voltage well and the second low voltage well.

10. (Original) The method of claim 8, further comprising ion implanting the substrate to adjust a threshold of the high voltage well, the first low voltage well and the second low voltage well.

11. (Previously Presented) The method of claim 9, further comprising:

forming a polysilicon layer over a gate oxide and the field oxide layer; and

removing a portion of the polysilicon layer to define a polysilicon gate for each of the high voltage well, the first low voltage well and the second low voltage well.

12. (Currently Amended) The method of claim 11, further comprising:

forming a fourth ion implantation protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the fourth ion implantation protective layer; and

ion implanting a P-body in the high voltage well of the first circuit device using the partially removed fourth ion implantation protective layer to allow ion implantation.

13. (Currently Amended) The method of claim 12, further comprising:

forming a fifth ion implantation protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the fifth ion implantation protective layer; and

ion implanting at least one N+ source/drain in the P-body, in the high voltage well of the first circuit device and in the first low voltage well of the second circuit device using the partially removed fifth ion implantation protective layer to allow ion implantation.

14. (Currently Amended) The method of claim 13, further comprising:

forming a sixth ion implantation protective layer over at least the field oxide layer and the polysilicon gates;

removing a portion of the sixth ion implantation protective layer; and

ion implanting at least one P+ source/drain in the P-body and in the first low voltage well of the second circuit device using the partially removed sixth ion implantation protective layer to allow ion implantation.

15. (Original) The method of claim 14, further comprising forming a passivation oxide layer over at least the field oxide layer and the polysilicon gates.

16. (Original) The method of claim 15, further comprising:

forming a plurality of vias through the passivation oxide layer to each of the N+ and P+ sources/drains;

forming a layer of metal over the passivation oxide layer and in the vias; and

removing a portion of the layer of metal over the passivation oxide layer to define a plurality of electrical interconnects.

17-46. Canceled.